工學碩士 學位論文

지우기 전류의 감소를 위한 PRAM cell 구조에 대한 연구

Study on the Novel PRAM cell structure for reducing reset current

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CONTENTS

Study on the Novel PRAM cell structure for reducing reset current

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Abstract

본 논문에서는 차세대 메모리인 상변화 메모리(Phase change random access memory)의 지우기 전류 감소를 위한 새로운 셀 구조에 관해 고찰하였다.

기록, 소거, 재생 속도, 재기록, 횟수 등을 포함한 성능에서 DRAM 급의 성능 특성을 가지며 소자구조 및 제작공정이 단순하여 정보저장 및 처리 용량대비 저가격화 달성이 용이한 상변화 메모리(PRAM)가 차세대 비휘발성 메모리로 주목 받고 있다. 그러나 상변화 메모리의 지우기 동작전류는 타 메모리 소자에 비해 큰 값을 나타내는 단점이 있어 상변화 메모리가 기존의 메모리 소자를 대체하기위한 경쟁력을 갖추기 위해서는

지우기 동작 전류를 낮추어야 한다. 상변화 메모리의 지우기 동작 전류를 낮추기 위해 상변화 물질, 발열전극 물질 및 셀 구조 변화 등의 연구가 진행 중이다. 그 중에서 셀 구조를 변형함으로써 지우기 전류를 줄여보고자 하는 연구가 이루어지고 있다.

본 연구는 PRAM의 지우기 전류를 줄이기 위해 상변화 물질 자체를 발열체로 사용하는 Pore형 PRAM 소자를 제작하여 소자 특성을 조사하였다. 또한 3차원 유한 요소 해석 프로그램을 이용하여 나노 스케일 PRAM의 GST박막의 두께에 따른 PRAM의 지우기 전류와 온도에 관해 조사하였고, 상변화 물질의 두께가 얇아질수록 지우기 전류가 증가하는 것을 알게 되었다. 지우기 전류의 증가를 막기 위해 SiO_2 열 방지층을 사용하는 새로운 구조의 PRAM cell을 제안하였고 또한 지우기 전류와 온도에 관한 조사를 하였다.

200 ㎚ 의 두께의 GST박막의 두께에서 기존의 구조와 새로운 구조의 PRAM을 비교하였을 때, 새로운 구조의 PRAM cell에서 온도는 536.60 ℃ 에서 817 ℃ 로 크게 증가하였고, 지우기 전류는 17.4 ㎃ to 13.7 ㎃ 로 감소하였음을 알 수 있었다. 이 결과는 새로운 구조의 PRAM cell이 열 방지층으로서 효과적으로 작용해 지우기 전류를 감소시킴을 알 수 있었다.

Chapter 1. Introduction

Recently, there is a strong demand on high speed, high density, low-power, and non-volatile memory to save data without a battery. Because use of memory devices which are PDA, cell phone, MP3, digital camera and so on is increasing. However there are some problems to use the flash memory over 75% of non-volatile memory market. The flash memory has lower speed than DRAM and difficult to integrate under 50 ㎚.

Now DRAM or SRAM is using for solving speed problem. But as two kinds of devices used, cost and power consumption was increased and structure was complicated. Therefore major semiconductor companies like Samsung, IBM, Intel, and Motorola have investigated FRAM(Ferroelectric RAM), MRAM(Magnetic RAM), and PRAM(Phase change RAM) instead of flash memory[1, 2]. Fig. 1.1 shows next generation non-volatile memories which are researched.

PRAM(Phase change random access memory) is one of the most promising candidates for next generation non-volatile memory due to its high speed memory operations, simple manufacturing process, and high density as nano-scale[3-5]. However, the PRAM needs time to research into electrical variation with structure change of device and degradation with integration

fabrication process. Particularly, as size and thickness of phase change material are as small as several tens nano scale, it is necessary to investigate the effect on operation of PRAM with electro-thermal property of phase change material.

To reduce the reset current of PRAM, studies are in progress such as development of phase-change materials, change of heater material, and decrease of TiN/GST contact size. However, there has been little research interest on the structural modification. Especially, Pore type PRAM which is using phase change material as heater was interested to reduce reset current.

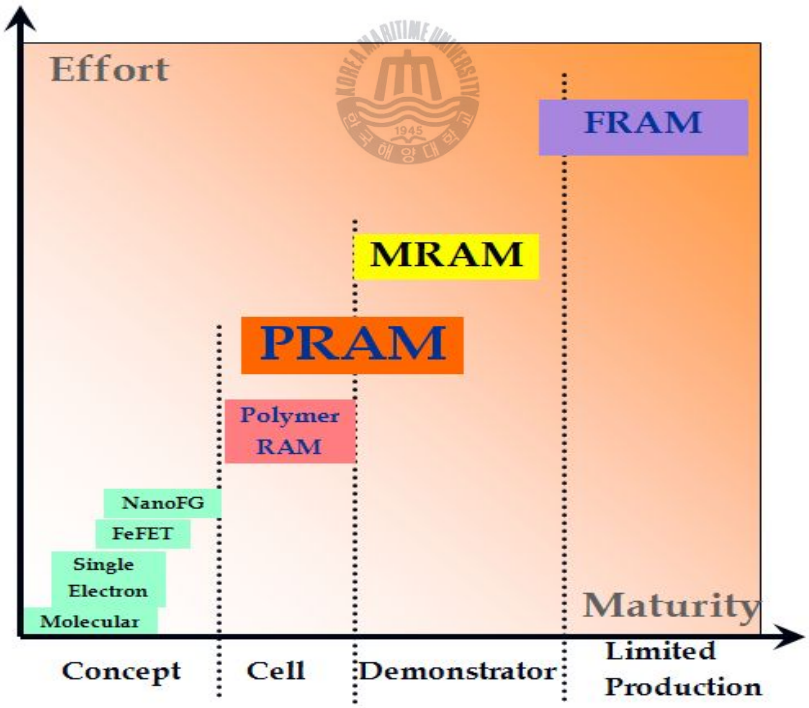


Fig. 1.1 Next generation non-volatile memories

In this paper, we investigated temperature and reset current of PRAM with thickness of GST thin film of nano scale PRAM using 3-D finite element analysis tool. And we proposed novel structure of PRAM unit cell with SiO_2 heat blocking layer. We investigated temperature and reset current of PRAM with SiO_2 heat blocking layer using 3-D finite element analysis tool.

Chapter 2. What is the PRAM

2.1 Definition and background of PRAM

PRAM(Phase change random access memory) is one of the promising nonvolatile memory owing to its large sensing signal, moderately fast writing time, endurance for repetitive writing and long data retention time[6].

Table 2.1 shows comparison characteristics with other memories. First thing is the switching time that makes PRAM, and other replacements for the flash memory, most interesting. PRAM's temperature sensitivity is perhaps its most notable drawback, one that may require changes in the production process of manufacturers incorporating the technology. PRAM's high speed, thousands of times quicker than conventional hard drives, makes it particularly interesting in nonvolatile memory roles that are currently performance-limited by memory access speed. PRAM devices also degrade with use, for different reasons than Flash, but degrade much more slowly. A PRAM device may endure around 100 million write cycles[7].

PRAM uses the unique behavior of chalcogenide glass, which can be switched between crystalline and amorphous states, with the application of heat. The PRAM technology being developed by Intel uses a class of materials known as chalcogenides

("kal-koj--uh-nyde"). Chalcogenides are alloys that contain an element in the Oxygen/Sulphur family of the Periodic Table (Group 16 in the new style or Group VI in the old style Periodic Table). The stoichiometry or Ge:Sb:Te element ratio is 2:2:5. When GST is heated to a high temperature (over 600℃), its chalcogenide crystallinity is lost. Once cooled, it gets frozen into an amorphous glass-like state and its electrical resistance becomes high.

Table. 2.1 Comparison characteristics with other memories

Memory Type	Speed	Power	Cost/Bit	Cycle life	Non-volatile	Endurance	Write Voltage
SRAM	Very High	Medium	High	Very High	No	10^{15}	~2-5V
DRAM	High	Low	Very Low	Very High	No	10^{15}	~2-5V
FLASH	Low	Medium	Low	Low	Yes	10^{6}	>12V
MRAM	High to Very High	Medium	High	Very High	Yes	10^{10}	~2-5V
FeRAM	High	Low	High	High	Yes	10^{12}	~2-5V
PRAM	High to Very High	Low to Very Low	Very Low	High to Very High	Yes	10^{13}	~2-5V
IDEAL	Very High	Very Low	Very Low	Very High	Yes	10^{15}	~2-5V

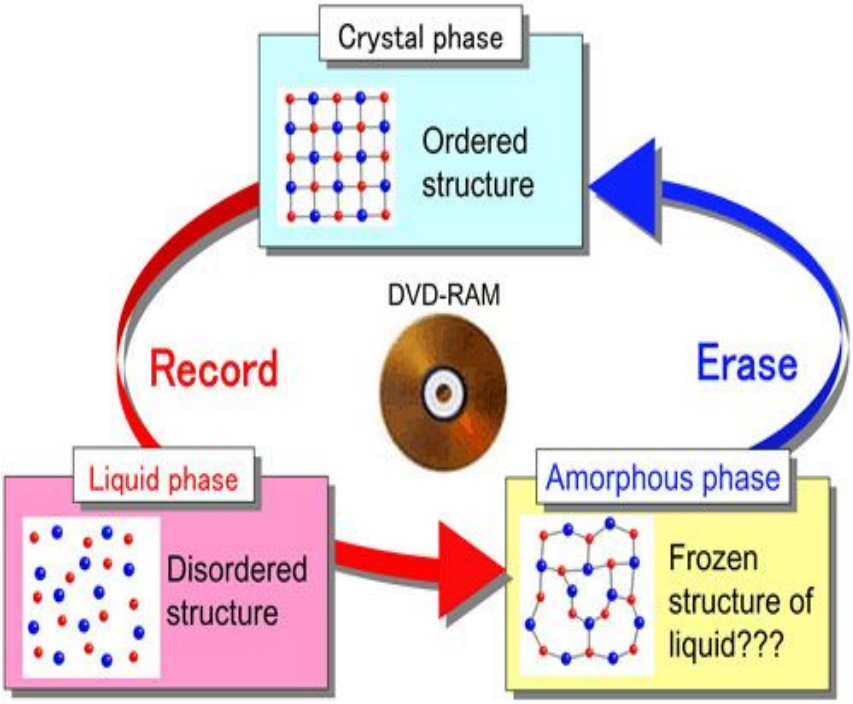


Fig. 2.1 Record/erase process in DVD-RAM

By heating the chalcogenide to a temperature above its crystallization point, but below the melting point, it will transform into a crystalline state with much lower resistance. The time to complete this phase transition is temperature-dependent. Cooler portions of the chalcogenide take longer to crystallize, and overheated portions may be remelted[8]. Chalcogenide is the same material as one used in re-writable optical media such as CD-RW[9]. Fig. 2. 1 shows phase transition and record/erase process in DVD-RAM. In those instances, the material's optical properties are manipulated, rather than its electrical resistivity, as chalcogenide's refractive index. Recent versions can achieve two

additional distinct states, effectively doubling its storage capacity.

PRAM is one of a number of new memory technologies that are attempting to compete in the non-volatile role with the almost universal Flash memory, which has a number of practical problems these replacements hope to address[10].

The properties of chalcogenide glasses were first explored as a potential memory technology by Stanford Ovshinsky of Energy Conversion Devices in 1960s. In September 1970 issue of Electronics, Gordon Moore—co-founder of Intel—published an article on the technology[11, 12]. However, material quality and power consumption issues prevented commercialization of the technology. More recently, interest and research have resumed as flash and DRAM memory technologies are expected to encounter scaling difficulties as chip lithography shrinks[13].

2.2 Theory of operation

Fig. 2.2 shows summary of the operation principle and characteristics of PRAM[14]. Basically, PRAM is based on the reversible phase transition between resistive amorphous and conductive crystalline states of chalcogenide[15].

In the amorphous phase, the material is highly disordered—here is an absence of regular order to the crystalline lattice. In this phase, the material demonstrates high resistivity and high reflectivity. In contrast, in the polycrystalline phase, the material

has a regular crystalline structure and exhibits low reflectivity and low resistivity[16].

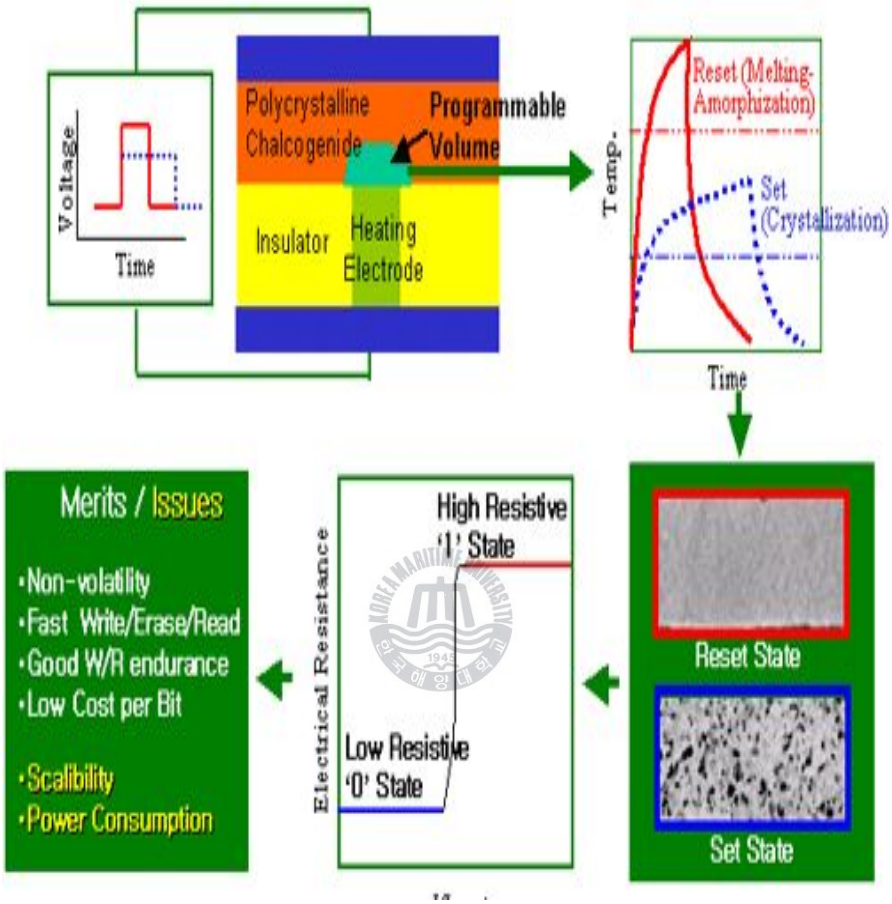


Fig. 2.2 Summary of the operation principle and characteristics of PRAM

In the PRAM, we are exploiting the difference in resistivity between the two phases of the material. This phase change is induced in the material through intense localized Joule heating caused by current injection[17, 18]. The end phase of the material is modulated by the magnitude of the injected current,

the applied voltage, and the time of the operation. The crystalline and amorphous states of chalcogenide glass have dramatically different electrical resistivity. The amorphous, high resistance state is used to represent a binary 0, and the crystalline, low resistance state represents a 1[19, 20].

As shown in Fig. 2.3, the write and read of the memory cell, including SET and RESET operations, are operated at the different I-V region.

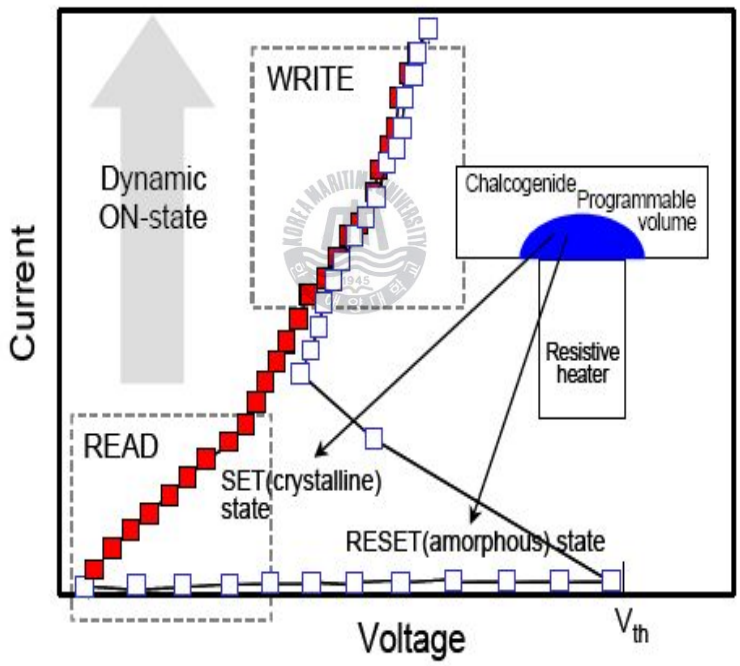


Fig. 2.3 I-V characteristics of PRAM

The write operation is performed at the dynamic on-state over Vth(threshold voltage) while the read operation is done at the low current level[21].

PRAM(Phase change random access memory) is one of the most promising candidates for next generation non-volatile memories because PRAM combines all the desirable characteristics such as DRAM, Flash, and SRAM. For PRAM, phase-change material $Ge_2Sb_2Te_5$ (GST) is transformed into crystalline (SET) or amorphous (RESET) state by applied current. Set and reset of cell are operated through heating using current pulse. In $I-V$ characteristic curve, as current pulse inserted into material over V_{th}, crystalline and amorphous state had dynamic resistance. And it is possible resistance heating. Therefore, as amplitude of inserted current pulse controls for temperature of material and annealing time, reset and set can transform. In the reading operation, little current applied to the bit line and electric potential of bit line compared with reference electric potential (V_{ref}) for deciding resistance state of PRAM. The reading operation is achieved only under V_{th} of PRAM as very low voltage.

Fig. 2.4 shows cell array of PRAM device. The structure of cell array is similar to the structure of DRAM, but it substitutes capacitor for phase change material. GST thin film is formed between top electrode (TE) and heater. Some current from writer driver insert into phase change material through bit line and top electrode contact for set and reset state.

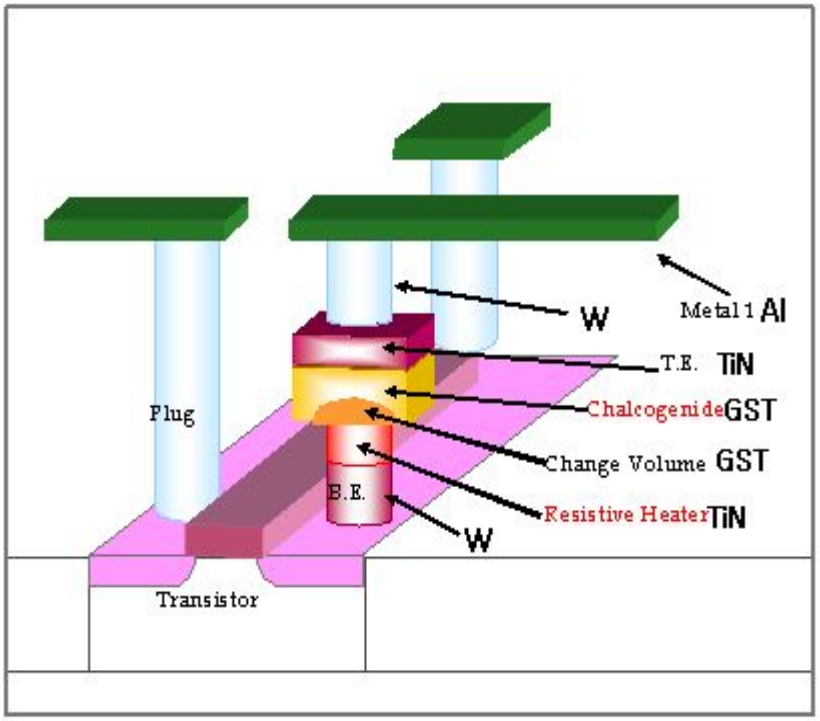


Fig. 2.4 Cell array of PRAM device

2.3 Method of reduction of reset current

Research period which is related to phase change memory is not so longer than other memory device. Especially in case of using phase change material as semiconductor memory device, phase transmission is happened by Joule's heat. And we need more research which is related to heat transmission and reset current for driving. Especially, the high reset current is one major obstacle to develop a nano scale PRAM. Recently research for reducing reset current have investigated using phase change

material, heater electrode, and cell structure. As follow three kind of methods show brief research to reduce reset current

① Development of alternative material of GST

: Alternative material of GST have to have lower melting temperature. Recently Se-Sb-Te material have been investigated instead of Ge-Sb-Te.

② Development of top and bottom electrode material

: Phase transmission which is happened by Joule's heat is generated between phase change material and heater electrode as top and bottom electrode. Recently TiAlN and SiGe which have high resistance and no problem to manufacture with GST thin film have been investigated.

③ Modification of cell structure

: Modification of cell structure which is made small contanct surface with GST makes efficient heat. Recently edge contanct cell and ring type contact for reduction reset current have been investigated.

2.4 Electromagnetic analysis

Non-volatile memory PRAM cell was modelled by the Poisson's equation or the Laplace's equation which were from the Maxwell's equations. These equations have a partial differentiation's equation with boundary condition. Getting a potential from these equations is almost impossible except for a special instance. Therefore

numerical analysis methods used to get a potential. Like these numerical analysis methods are finite difference method, boundary element method and so on. In these of methods, finite element method uses in public. Recently most of the commercialization programs are on the basis of finite difference method. In this paper, commercial program MagNet, ThermNet were used to analyze.[22]

The Poisson's equation is easy to get from differentiation of Gauss's law.

Differential-equation form of Gauss's law is,

$$\nabla \cdot D = \rho$$

From definition of D,

$$D = \epsilon E$$

Using the potential gradient, the electric field density is,

$$E = -\nabla V$$

From these equations we got this,

$$\nabla \cdot D = \nabla \cdot (\epsilon E) = -\nabla \cdot (\epsilon \nabla V) = \rho$$

Poisson's equation is,

$$\nabla \cdot \nabla V = -\rho/\epsilon$$

Electric charges in motion constitute a current and the current density J is,

$$J = \rho v$$

Differential form of the continuity equation is,

$$\nabla \cdot J = -\frac{\partial \rho}{\partial t}$$

As the electric field inserted material, μ is mobility of material,

$$\nabla \cdot J = -\rho \mu E$$

The relationship between J and E for metallic conductor is specified by the conductivity σ (sigma),

$$J = \sigma E$$

From these results the boundary conditions are defined at the analysis region

$$E \cdot n = 0,\ H \cdot n = 0$$

$$E \times n = 0,\ H \times n = 0$$

$$\frac{\partial \phi}{\partial n} = 0,\ \frac{\partial V}{\partial n} = 0$$

2.5 Thermal analysis

PRAM cell needs thermal analysis of memory device due to phase transmission to crystalline or amorphous state by Joule's heat. FEM (finite element method) and FDM (finite difference method) are being used for solving equations which are related with conservation of mass, momentum, and energy. Heat is one of energy which moves from high temperature to low temperature. It is measured by heat flow rate, heat flux, and temperature. Heat

flow rate is transferred heat per hour.

Heat flow rate by heat conduction is inversely proportional to multiplication of vertical surface of heat flow and temperature inclination. For instance, heat flow where to x by the Fourier's law is,

$$Qx = -kA\frac{dT}{dX} \qquad \text{(Heat flow rate)}$$

$$qx = \frac{Q}{A} = -k\frac{dT}{dX} \qquad \text{(Heat flux)}$$

The proportional factor k is thermal conductivity of material and always has a positive result. Heat which transfers by material express location and time function. Therefore thermal conduction equation is,

$$\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x}) = \rho c\frac{\partial T}{\partial t}$$

But in the steady state temperature does not depend on time. Therefore,

$$k_{xx}\frac{d^2T}{dx^2} = 0$$

This equation is 1 dimension thermal conduction equation. Thermal equation of 2 and 3 dimension are,

$$k_{xx}\frac{d^2T}{dx^2} + k_{ww}\frac{d^2T}{dy^2} = 0$$

$$k_{xx}\frac{d^2T}{dx^2} + k_{ww}\frac{d^2T}{dy^2} + k_{cc}\frac{d^2T}{dz^2} = 0$$

In many case, temperature variation of material is changed by time and location. Also boundary condition is changed by time. Transient analysis is that temperature and heat flow state of solid are time and location function. In case of changing boundary condition by time, it applies. Variation rate with time of temperature is still due to transient state. Hence, equation is,

$$\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x}) = \rho c\frac{\partial T}{\partial t}$$

This equation is thermal conduction equation of 1 dimension transient state . Thermal conduction of 2 and 3 dimension equations are,

$$k_{xx}\frac{d^2T}{dx^2} + k_{ww}\frac{d^2T}{dy^2} = \rho c\frac{\partial T}{\partial t}$$

$$k_{xx}\frac{d^2T}{dx^2} + k_{ww}\frac{d^2T}{dy^2} + k_{cc}\frac{d^2T}{dz^2} = \rho c\frac{\partial T}{\partial t}$$

$$\frac{d^2T}{dx^2} + \frac{d^2T}{dy^2} + \frac{d^2T}{dz^2} = \frac{\rho c}{k}\frac{\partial T}{\partial t}$$

Chapter 3. Experimental

3.1 Fabrication procedure

Fig. 3.1 shows a schematic cross section of the fabricated PRAM device which is in a pore-style configuration. The fabrication procedure of the conventional PRAM device is as follows.

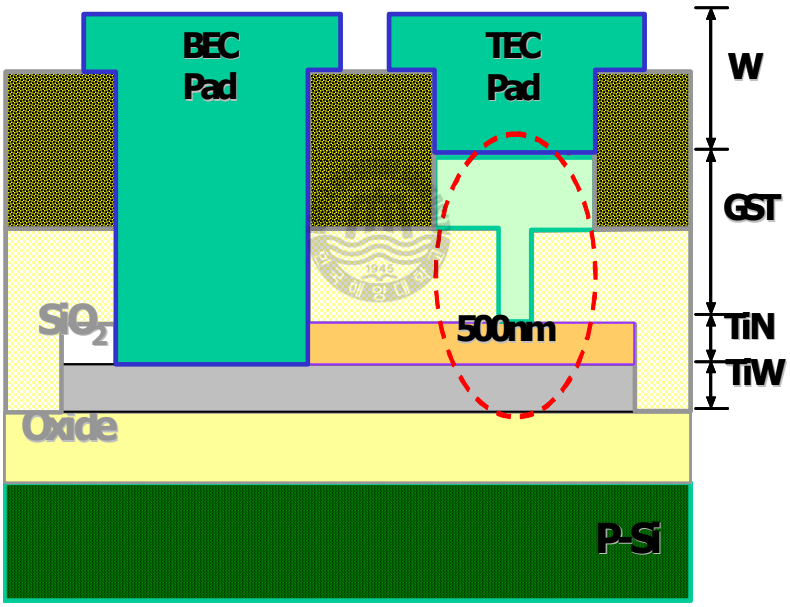


Fig. 3.1 Schematic diagram of a cross section of conventional PRAM unit cell

First, a bottom electrode (BE) of TiN/TiW was formed on SiO_2/Si substrate, on which SiO_2 insulation layer of 100 ㎚ was deposited by a plasma-enhanced chemical vapor deposition.

Active pores for the contact between the phase-change material and the BEC were patterned into on oxide layer, in which the contact size was defined to be 500 ㎚. Then, GST was deposited RF magnetron sputtering method, respectively. The thickness of a deposited film was about 400 ㎚. Finally, top electrode contact (TEC) of W was formed after a via contact was patterned.

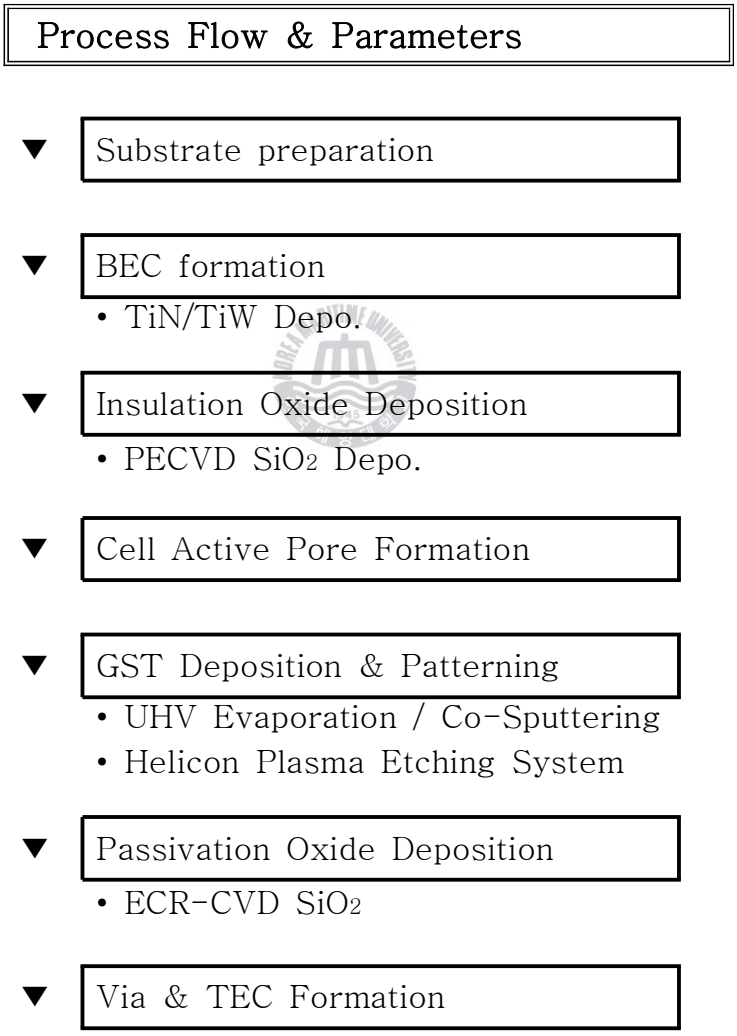


Fig. 3.2 Flow chart of fabrication procedure

Fig. 3.2 shows briefly fabrication of memory device as flow chart. It makes easy to understand PRAM of fabrication procedure. And Fig. 3.3 shows Order of PRAM test cell fabrication procedure.

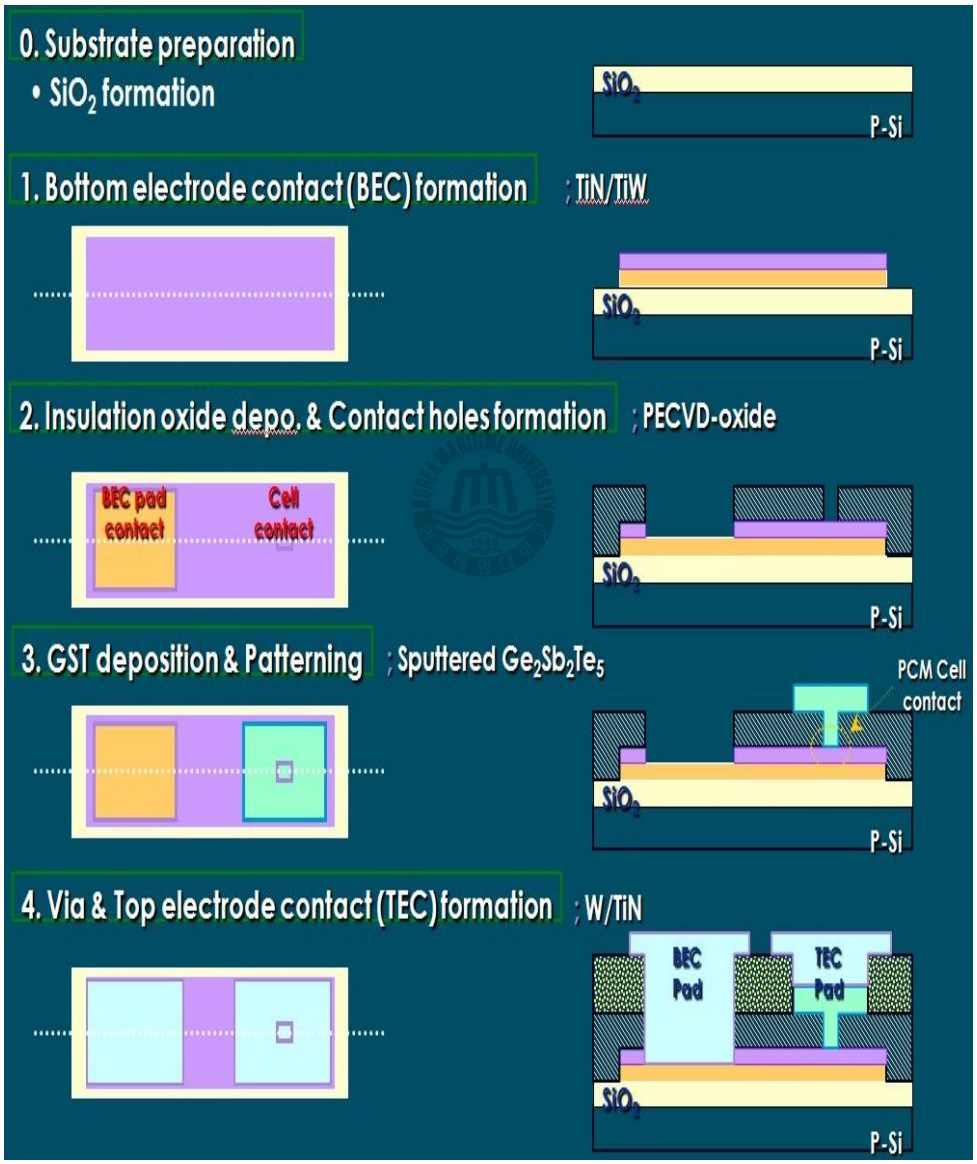


Fig. 3.3 Order of PRAM test cell fabrication procedure

For investigating characteristics of fabricated PRAM cell, HP 8110A, HP 4145B, Digital oscilloscope, and Probe station was used. Fig. 3.4 shows measurement system for fabricated PRAM cell.

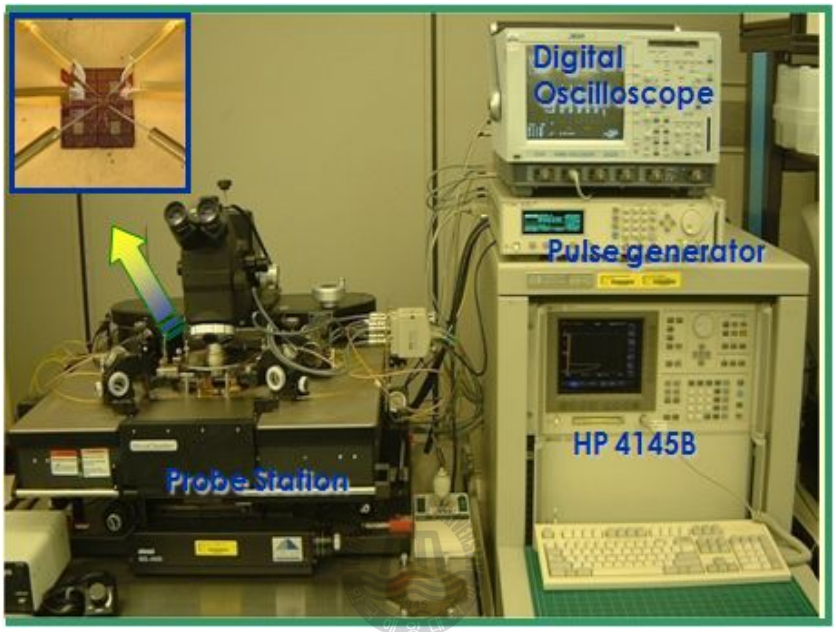


Fig. 3.4 Measurement system for fabricated PRAM cell

The operation behaviors of the fabricated devices were characterized by the electrical measurement system, in which the voltage and current pulses for set and reset operations were provided by a programmable pulse generator (HP 8110A). The resistance across the memory device at each operation was measured by a semi-conductor parameter analyzer (HP 4145B) via steady-state current-voltage (I-V) tests in a sampling mode.

3.2 Finite element analysis

For accomplishment better goal, it needed that a copying PRAM cell, which is for measuring magnetic field distribution, to manufacture 3-D numerical analysis model. And electro-thermal properties of copying PRAM cell suggested temperature distribution at PRAM cell of generated Joule's heat through 3-D electromagnetic field simulation. For electromagnetic field and thermal transform analysis, basic theory and model were introduced below. This study was simulated temperature and reset current of PRAM device using element analysis. Since PRAM device should be manufactured through a lot of unit process, very high cost and long process time are serious problems for confirming operational characteristic.

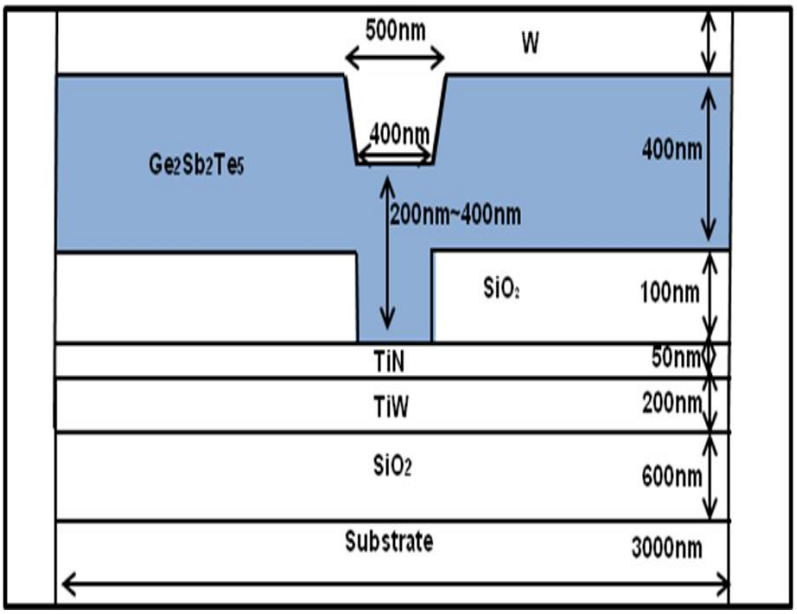


Fig. 3.5 Schematic diagram of PRAM unit cell

Therefore, simulation of performance characteristic should be employed for PRAM unit cell prior to fabricate PRAM device. This study was simulated temperature and reset current of PRAM device using finite element analysis. 2-D schematic diagram of unit cell as shown in Fig. 3.5 was prepared to build an analysis model of PRAM.

Fig. 3.6 is an finite element analysis model image of PRAM cell for precision electro-thermal analysis. 3-D finite element analysis model was constructed using MagNet and ThermNet which are commercial electro-magnetic field and thermal analysis tool.

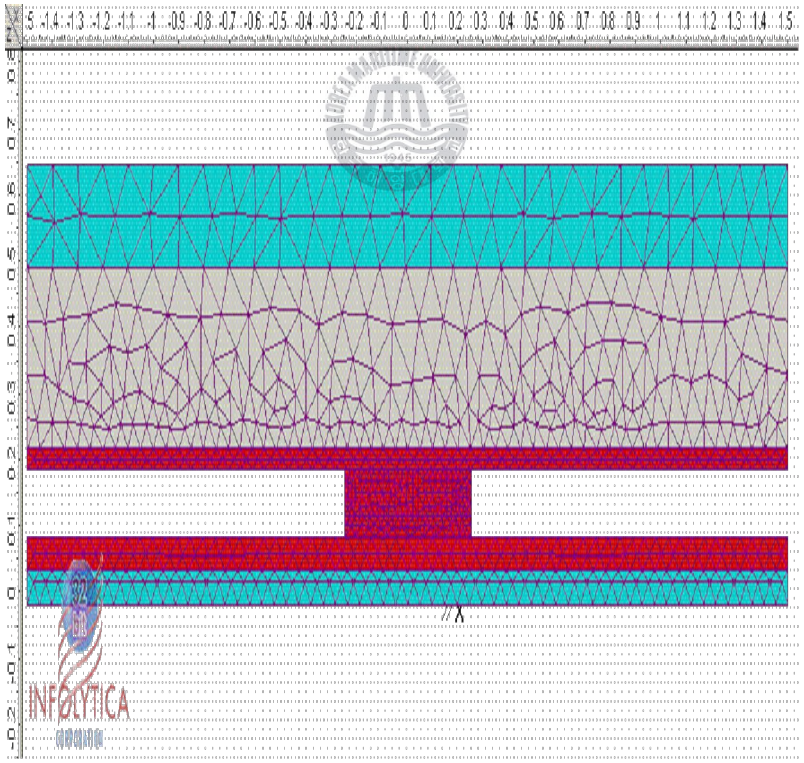


Fig. 3.6 Finite element model of PRAM unit cell

The heat transfer equation is solved with fixed temperature boundary condition. The temperature of outside of unit cell is 85 ℃ and time step for transient analysis is 20 ns. The material parameters are summarized in Table 3.1.

Table. 3.1 Material parameters

Material	Electrical Conductivity (1/Ω·m)	Thermal Conductivity (J/cm·K·s)	Specific heat (J/㎤·K)	Density (g/㎤)
W	$1.75x\ 10^{7}$	1.78	2.58	19.3
GST (Crystalline)	$2.4x\ 10^{4}$	0.016	1.2	6.2
GST (Amorphous)	$3.0x10^{1}$	0.004	1.2	6.2
TiN	$1.0x\ 10^{6}$	0.13	3.24	5.4
TiW	$1.43x\ 10^{6}$	0.6	2.09	14.3
SiO_2	$1.0x\ 10^{-14}$	0.014	3.1	2.33

Chapter 4. Results and discussion

In this paper, we fabricated the Pore type PRAM device and electrical characteristics. And we have investigated temperature and reset current of PRAM unit cell with thickness of GST thin film of nano scale PRAM using 3-D finite element analysis tool. For higher performance, PRAM must resolve reduction of reset current.

For reduction of reset current, we proposed novel structure of PRAM unit cell with a heat blocking layer and investigated electro-thermal characteristics of high density PRAM with a heat blocking layer.

4.1 Electro-thermal characteristics of PRAM cell

4.1.1 Electrical property

Fig. 4.1 illustrates fully processed Pore type PRAM unit cell using $Ge_2Sb_2Te_5$ film. The GST film was successfully integrated into pore type unit cell without any processing issues. And we investigated electrical characteristics of PRAM unit cell using fabricated pore type PRAM unit cell.

Fig. 4.2 shows programming curves of the fabricate PRAM unit cell when the current was applied.

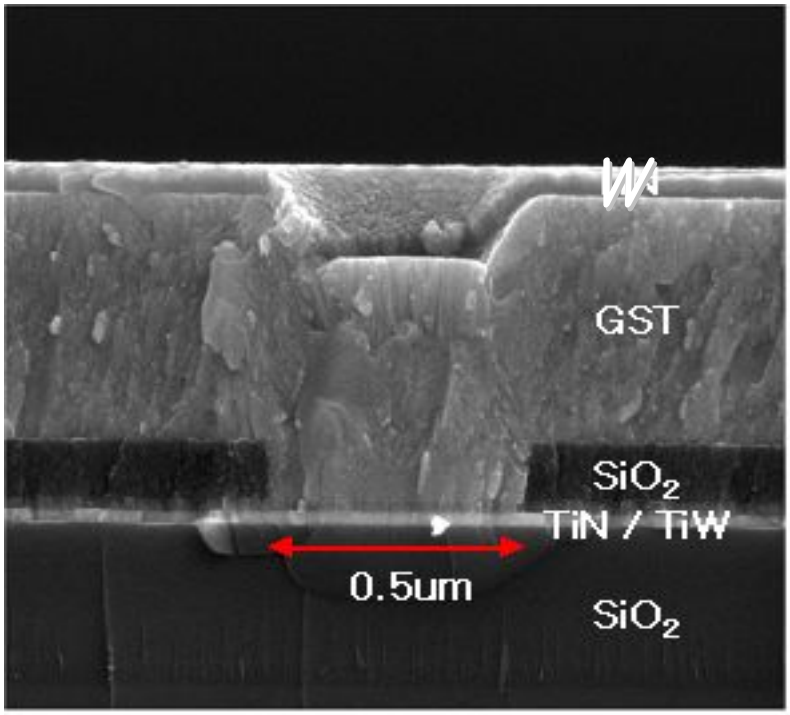
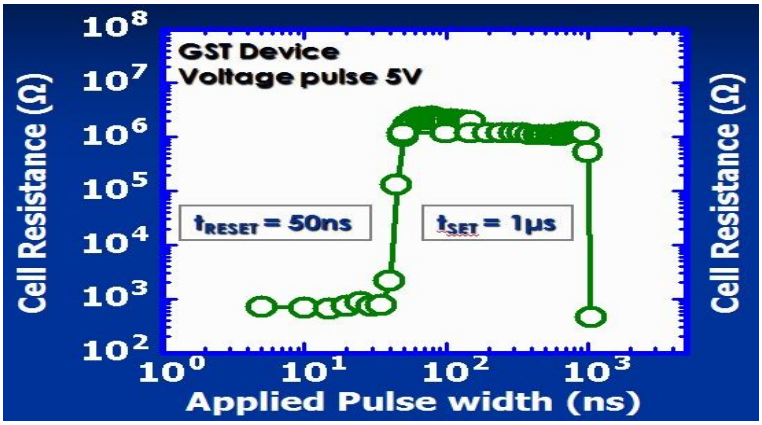
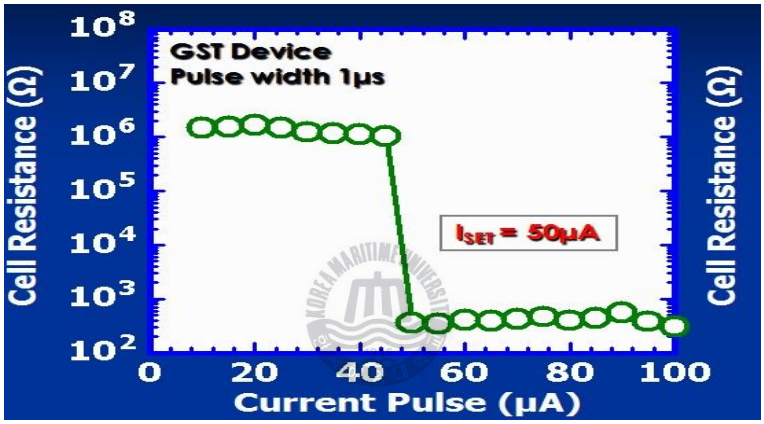


Fig. 4.1 SEM image of fabricated PRAM device

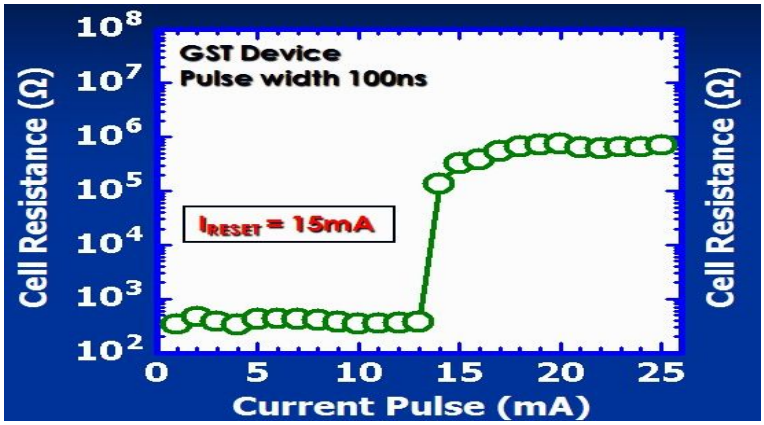
Fig. 4.2 shows (a) memory operations(set/reset) which explains that faster crystallization time can contribute to higher speed set operation, (b) programming curves for set and (c) programming curves for reset. In the Fig. 4.2(b), as curret was applied from 0 to 100 ㎂ with 1 ㎲ pulse width, the cell resistance decreased at 50 ㎂. It means set current 50 ㎂-1 ㎲ for crystalline state. In the Fig. 4.2(c), as current was applied from 0 to 25 ㎃ with 100 ㎱ pulse width, the cell resistance highly increased at 15 ㎃. It means the reset current 15 ㎃-100 ㎱ for amorphous state.



(a) Memory operations (set/reset)



(b) Programming curves for set



(c) Programming curves for reset

Fig. 4.2 Programing curves of the fabricate PRAM

4.1.2 Electro-thermal analysis

First of all, we have analyzed temperature distribution of PRAM unit cell by reset current to test reliability of commercial electro-thermal analysis tool used in simulation. PRAM is operated reset state with a short high current pulse, local part of phase change material is instantly melted and cooled rapidly at over melting temperature for amorphous. Melting temperature of Phase change material $Ge_2Sb_2Te_5$ used in this study is 632 ℃[24, 25].

The phase-change material reaches 704℃ slightly higher than melting temperature and becomes amorphous if the PRAM is under RESET operation. Reset current pulse of phase change memory cell as shown Fig. 4.3 and 4.4 are generally 15 ㎃-100 ㎱. Therefore, we numerically calculated ohmic loss and temperature of conventional PRAM unit cell model, which were gained by applying reset current of value 15 ㎃-100 ㎱ and it was compared with the temperature of actually fabricated PRAM. Fig. 4.3 shows that reset current applied through the top electrode concentratedly flows toward the outside of heater through phase change material.

Fig. 4.4 shows distribution of temperature with reset current of conventional PRAM cell model. As 15 ㎃-100 ㎱ reset current applied to constructed PRAM cell model, heat transferred to phase change material.

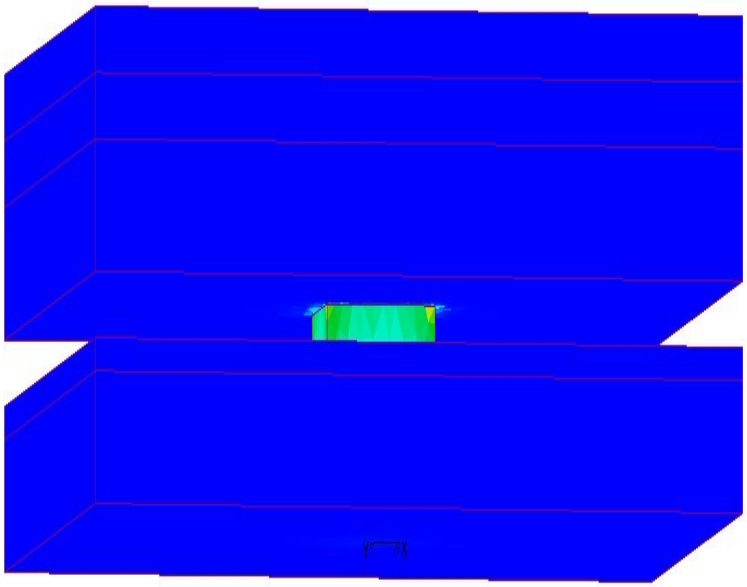


Fig. 4.3 Ohmic loss of conventional PRAM unit cell

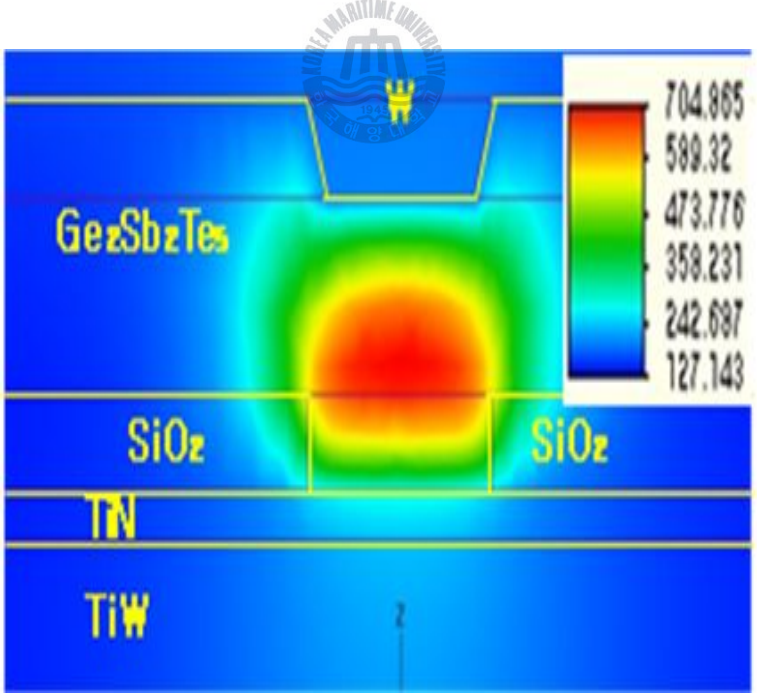


Fig. 4.4 Temperature distribution of conventional PRAM unit cell

And it completely melted at 704℃ and became amorphous structure. As shown in the figure, temperature of the established finite element analysis model and temperature of the actually manufactured device are equivalent.

4.1.3 Effect of thickness of $Ge_2Sb_2Te_5$

As PRAM became high density as nano scale, size and thickness of each material were smaller and thinner. In a given pore size, we reduced GST thin film thickness as low as possible.

As thickness of GST film became thin from 400 ㎚ to 300 ㎚, reset current increased a bit but did not affect memory cell operation so much. But as thickness of GST thin film became thin 300 ㎚ and 150 ㎚, reset current abruptly increased and memory cell operation did not work as normal.

Fig. 4.5 shows reset current of conventional PRAM unit cell with GST thin film thickness. In this figure, reset current is that proper reset current can melt phase change material for amorphous state. The standard temperature is 704.86 ℃ which is slightly higher than melting temperature at 300 ㎚ GST thin film thickness. As thickness of GST thin film got thin from 300 ㎚ to 200 ㎚, reset current increased from 15 ㎃ to 17.4 ㎃.

Fig. 4.6 shows temperature distribution of conventional PRAM unit cell at 200 ㎚ GST thin film thickness. Moreover in this figure, the heat source was generated in the middle of phase

change material GST.

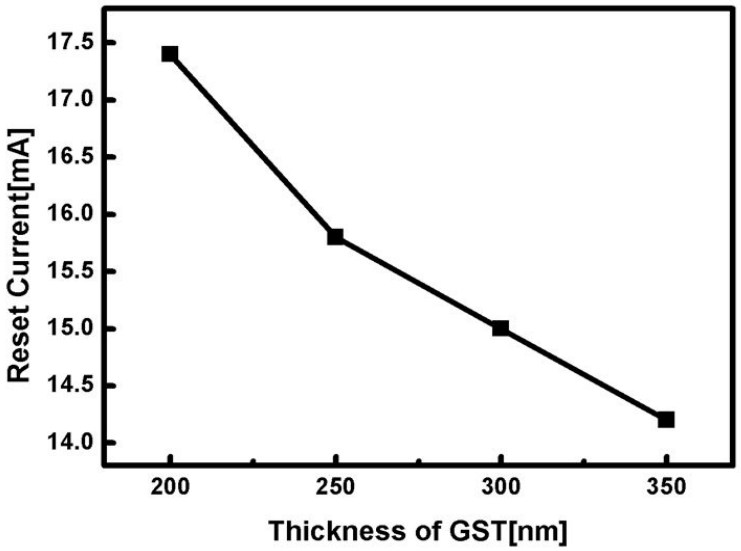


Fig. 4.5 reset current of conventional PRAM unit cell with thickness of GST thin film

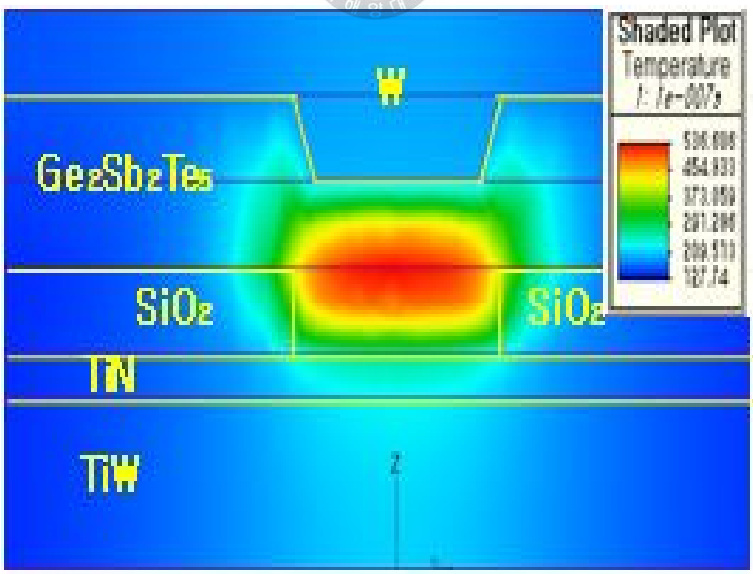


Fig. 4.6 Temperature distribution of conventional PRAM unit cell at 200 ㎚ GST thin film thickness

Therefore, we have throughly investigated the function failure of PRAM unit cell of 200 ㎚ GST thickness. Fig. 4.7 shows temperature of PRAM cell with thickness of GST thin film by applying reset current value 15 ㎃ and 100 ㎱ through simulation. As shown in Fig. 4.7, as thickness of GST thin film became thin from 400 ㎚ to 300 ㎚, temperature decreased about 70℃ but it didn't affect operation. But as thickness of GST thin film became thin from 300 ㎚ to 200 ㎚, temperature abruptly decreased from 704.86 ℃ to 536.60 ℃.

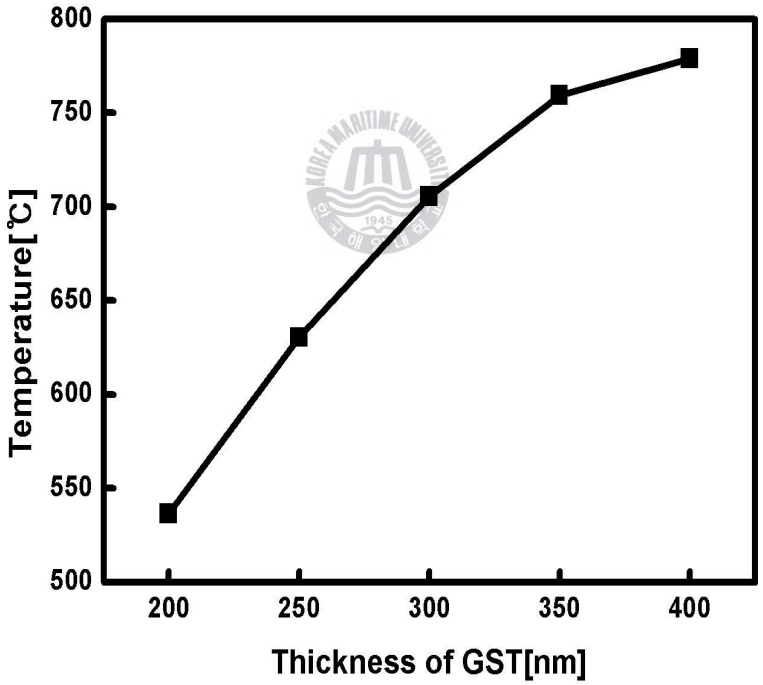


Fig. 4.7 Temperature of conventional PRAM unit cell with thickness of GST thin film

We have investigated the reason why temperature decreased and reset current increased, as thickness of GST got thin. For this investigation, electrical conductivity, specific heat, and thermal conductivity of top electrode were changed. As thermal conductivity of top electrode decreased, let us know that temperature increased by this investigation. Therefore, the heat which was generated by thinned GST given off through top electrode easily.

Fig. 4.8 shows temperature distribution, as thermal conductivity of top electrode decreased. For protecting heat from giving off with keeping thinned thickness, novel structure PRAM cell was proposed.

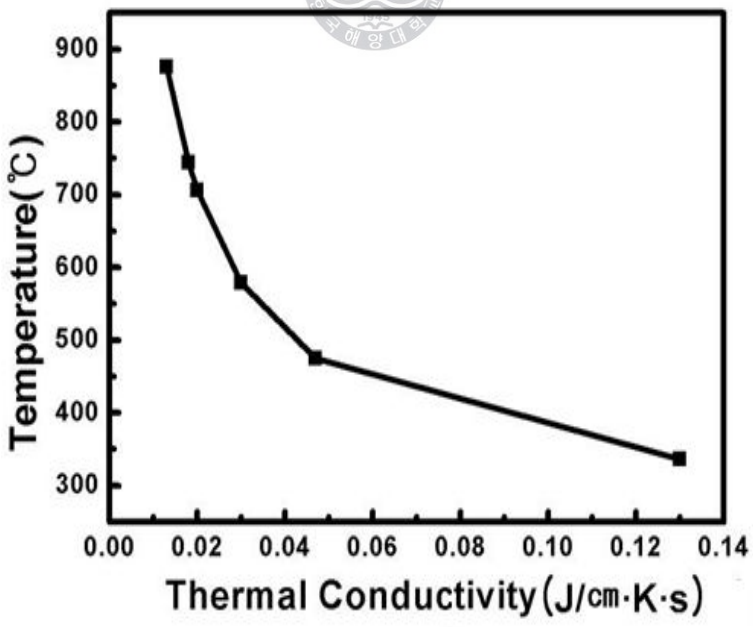


Fig. 4.8 Temperature distribution with thermal conductivity

4.2 Effect of novel structure PRAM unit cell

4.2.1 Finite element analysis model of novel structure

We have thoroughly investigated the decreasing of temperature of 200 ㎚ thickness of GST thin film and found that the severe heat loss occurred at W top electrode. In the case of 200 ㎚ thickness of GST thin film, a heat rapidly transferred to top electrode before melting temperature due to thickness of GST thin film. A heat which contacted with top electrode transferred easily to outside and temperature decreased and reset current increased. Therefore, we investigated a method to protect decreasing temperature for competitive low-power and nonvolatile memory at 200 ㎚ thickness of GST thin film.

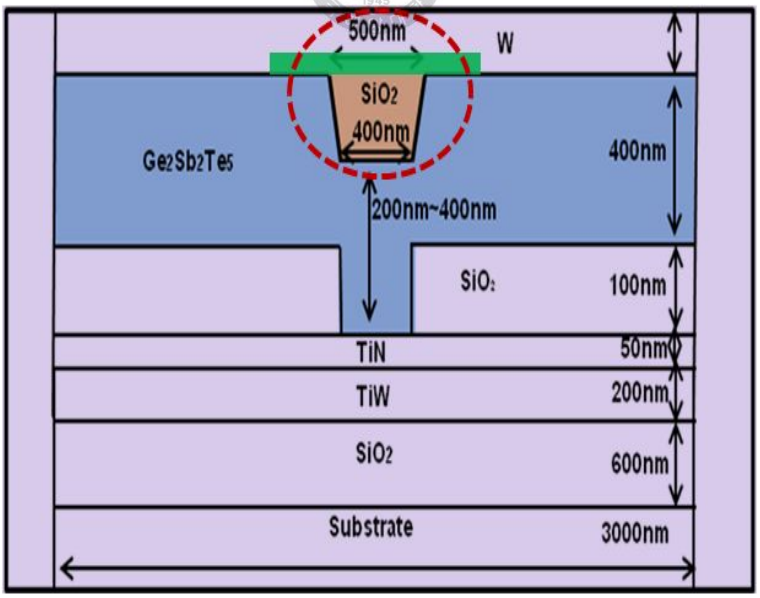


Fig. 4.9 Schematic diagram of novel structure PRAM unit cell with SiO_2 blocking layer

For this, novel structure PRAM unit cell was proposed. Fig. 4.9 shows novel structure which deposited SiO_2 blocking layer instead of part of top electrode for reduction reset current. The proposed novel structure PRAM unit cell deposited SiO_2 as blocking layer between top electrode and phase change material. The SiO_2 blocking layer which is dielectric layer can protect the heat to give off through top electrode. It means this method can increase temperature and decrease reset current.

4.2.2 Electro-thermal analysis model

Fig. 4.10 shows temperature of PRAM with SiO_2 blocking layer of 200㎚ GST thin film by appling 15 ㎃-100 ㎱ reset current.

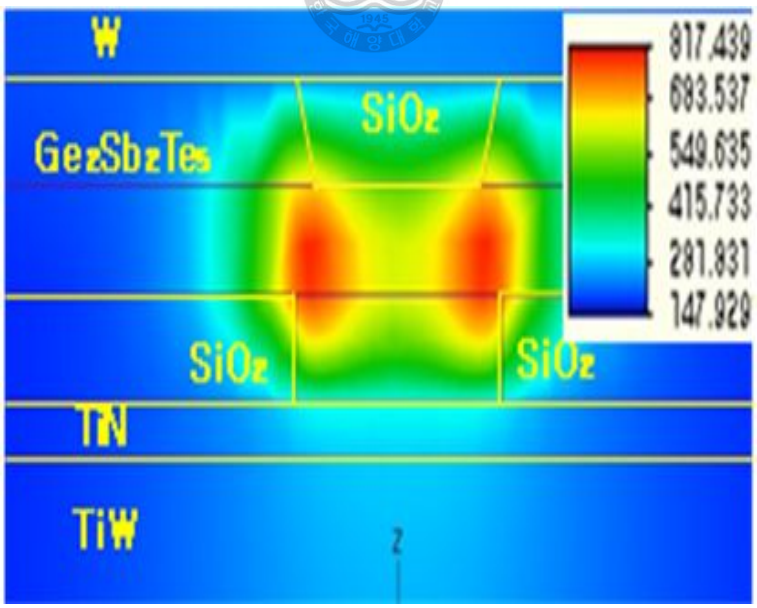
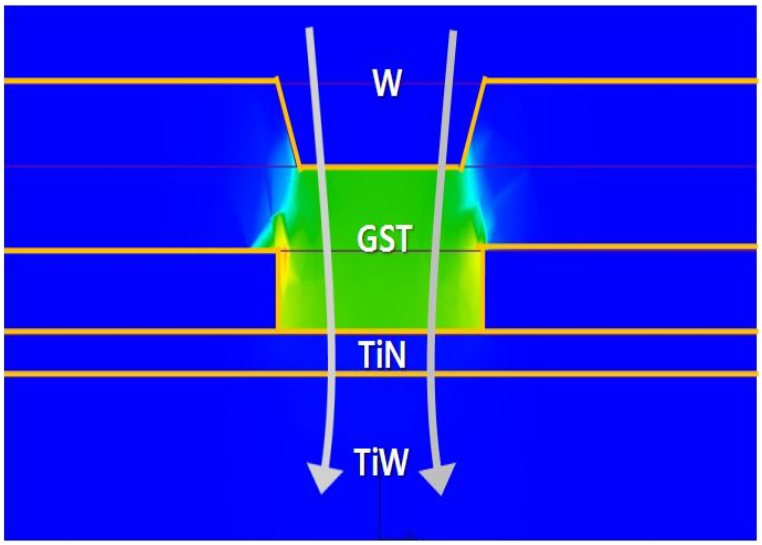


Fig. 4.10 Temperature distribution of novel structural PRAM with SiO_2 blocking layer

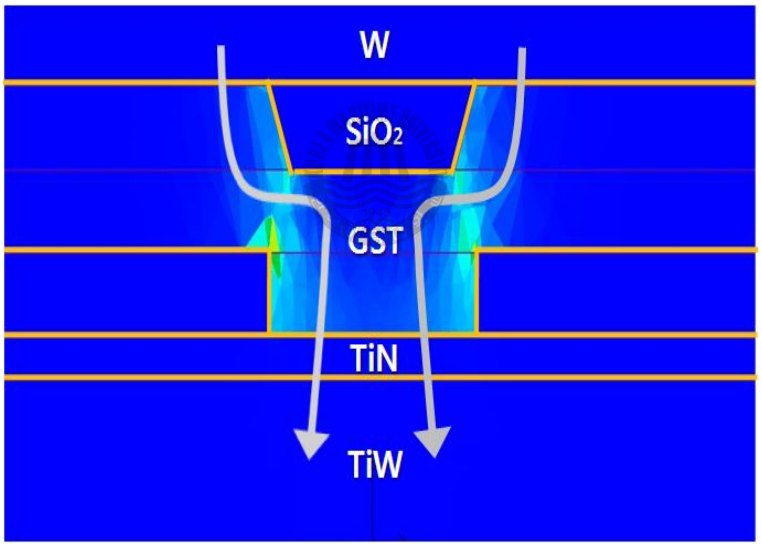
As shown in the figure, temperature of GST was increased over 817 ℃ and the programmable volume is center of GST. It was reason of increasing temperature of phase change material compared with the conventional structure.

Fig. 4.11 shows the ohmic loss and current flow of PRAM unit cell model. In conventional structure, the ohmic loss which is source of heat was generated at the middle of GST thin film area over TiN electrode. But in the case of novel structure PRAM, the ohmic loss was generated at almost GST phase change material. And the power (ohmic loss) of GST thin film highly increased compared with conventional PRAM. Power (ohmic loss) for reset state is proportional to reset current(I) and cell resistance(R): $P \propto I^2R$. As same current applied to each structure, power of novel structure is higher than conventional structure due to the high resistance of GST thin film. The reason why novel structure PRAM has high resistance is the path of current flow which was changed by SiO_2 blocking layer of novel structure PRAM.

Fig. 4.11 (a) shows that a reset current of conventional structure from the top electrode flowed to the bottom electrode through the center of a GST thin film. In the conventional structure, the ohmic loss generated at middle of GST. But, in novel structure, reset current flows from the outside of the SiO_2 blocking layer to bottom electrode as shown Fig. 4.11 (b).



(a) Conventional PRAM unit cell



(b) Novel structure PRAM unit cell

Fig. 4.11 Current flow and ohmic loss

Because of changed current path, the resistance abruptly increased and the ohmic loss generated at almost GST area. Therefore, novel structure PRAM has a much larger heat source

area compared with the conventional PRAM.

Fig. 4.12 shows comparison of reset current and temperature of novel structure PRAM and conventional structure PRAM at 200 ㎚ thickness of GST thin film. In comparison with conventional PRAM at 200 ㎚ GST thin film thickness, temperature of novel structure PRAM highly increased 280.76 ℃ from 536.60 ℃ to 817 ℃. This result shows that novel SiO_2 blocking layer of PRAM successfully protected heat to give off to top electrode.

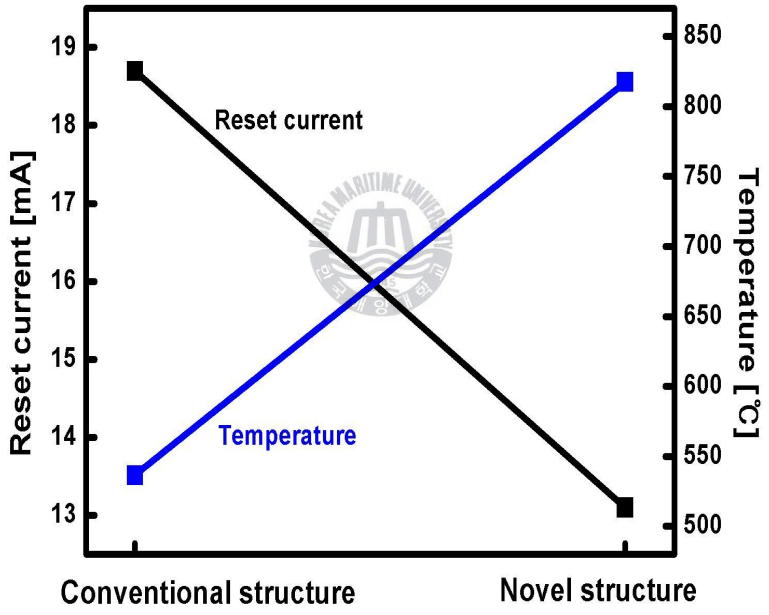


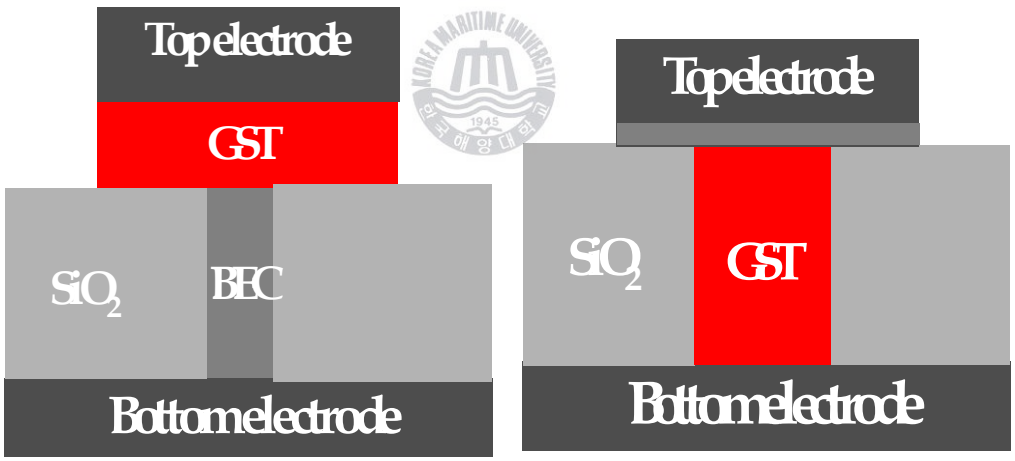
Fig. 4.12 Temperature and reset current of PRAM unit cell with each structure

The calculated reset current of novel structure of PRAM unit cell is 13.7 ㎃. The PRAM with SiO_2 heat blocking layer has 30% smaller reset current than the conventional PRAM device.

4.3 Effect of heat blocking layer in planar type PRAM

4.3.1 Finite element analysis model

After used SiO_2 heat blocking layer, we got good effect to pore type PRAM cell. PRAM cell has other type PRAM which has used in a variety of research area. Therefore, we applied SiO_2 heat blocking layer to planar type PRAM cell. Fig. 4.13 shows structure of PRAM unit cell. In the pore type PRAM cell, heat is generated in the middle of GST. However, in the planar type PRAM unit cell, heat is generated between GST and bottom electrode contact.



(a) Planar type (b) Pore type

Fig. 4.13 Structure of PRAM unit cell

2-D schematic diagram of unit cell as shown in Fig. 4.14 was prepared to build an analysis model of planar type PRAM cell.

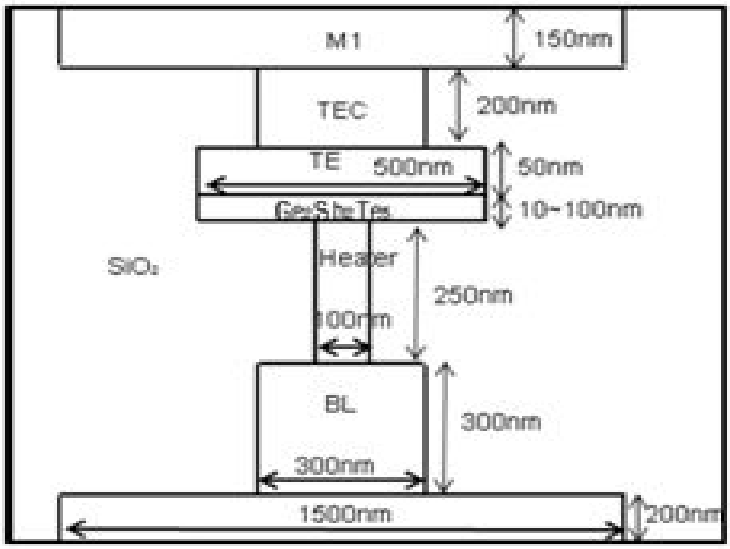


Fig. 4.14 Schematic diagram of PRAM unit cell

Fig. 4.15 shows an finite element analysis model image of planar type PRAM cell for precision electro-thermal analysis.

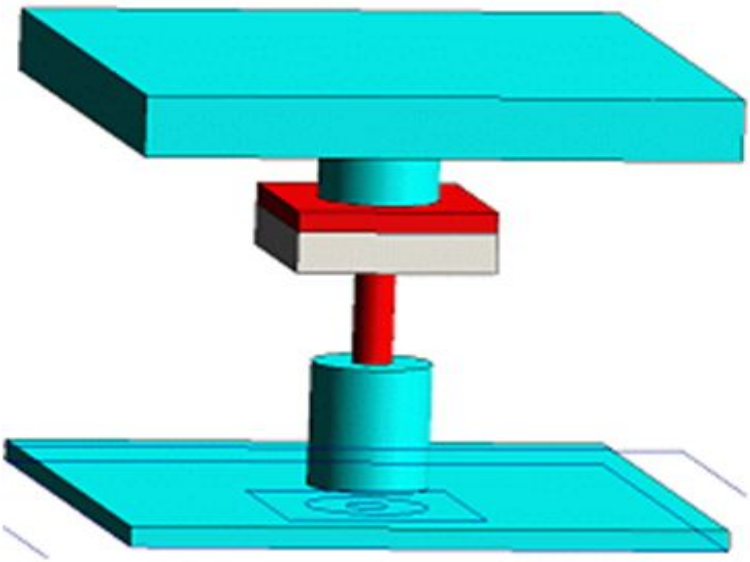


Fig. 4.15 Finite element model of planar type PRAM cell

As 2 ㎃-50 ㎱ reset current applied to planar PRAM cell model, heat which was generated between phase change material and heater electrode contact surface transferred to phase change material. And as shown Fig. 4.16, it completely melted at 730℃ and became amorphous structure.

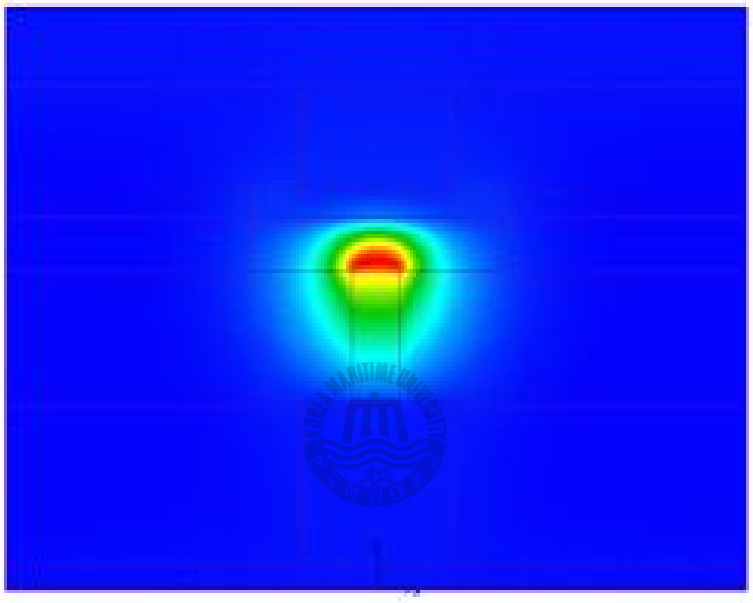


Fig. 4.16 Temperature distribution of planar type PRAM cell

As thickness of GST thin film of PRAM cell model changed from 100 ㎚ to 10 ㎚, we investigated temperature of PRAM cell model with 2 ㎃-50 ㎱ reset current. Fig. 4.17 shows temperature and reset current of planar PRAM cell with thickness of phase change material. As thickness of GST thin film became thin from 100 nm to 50 nm, temperature decreased a bit but did not affect so much memory cell operation. But as thickness of GST thin film

became thin 50 nm and 10 nm, temperature abruptly decreased and memory cell operation did not work as normal.

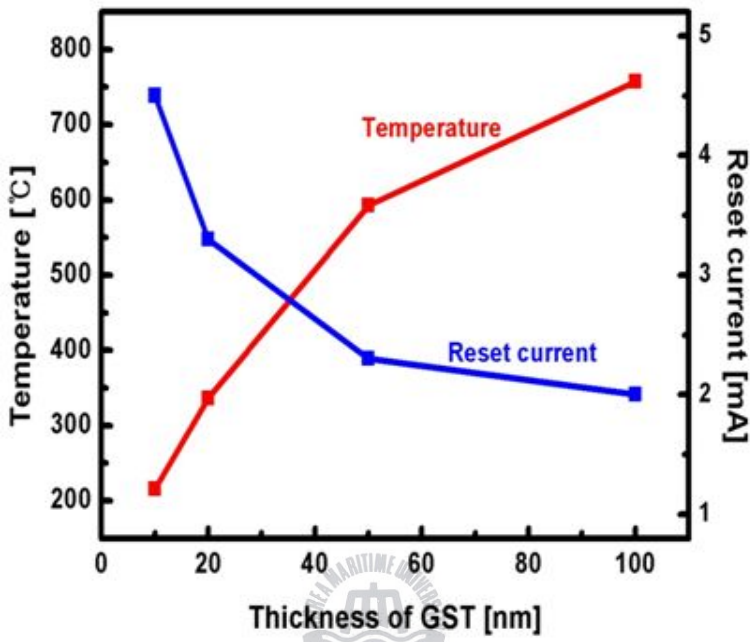


Fig. 4.17 Temperature and reset current of planar type PRAM cell with thickness of GST

As show Fig. 4.17 reset current increased 125% and temperature decreased 79.5%. Therefor, we applied heat blocking layer to planar type PRAM cell with 10 ㎚ thickness of GST.

4.3.2 Effect of heat blocking layer

Fig. 4.18 shows planar type PRAM cell using SiO_2 heat blocking layer. In conventional planar type PRAM cell case, 50nm thickness of TiN top electrode was deposited on GST thin film.

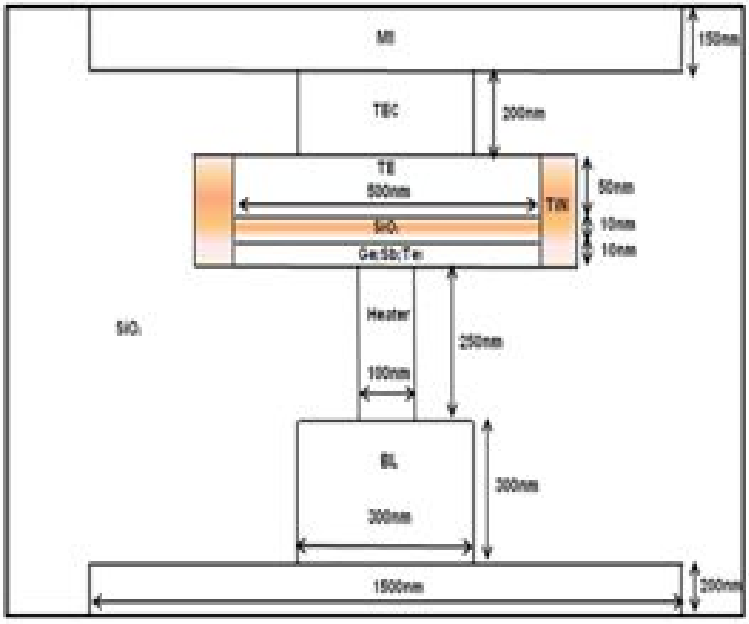
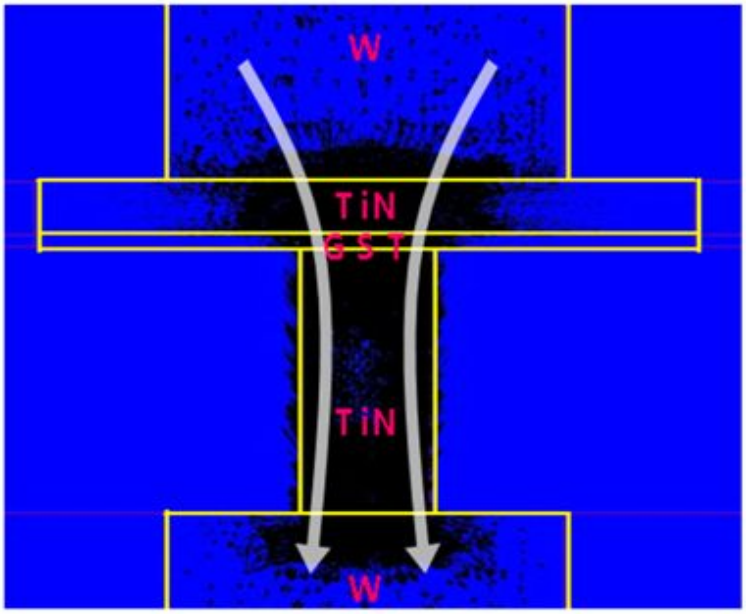


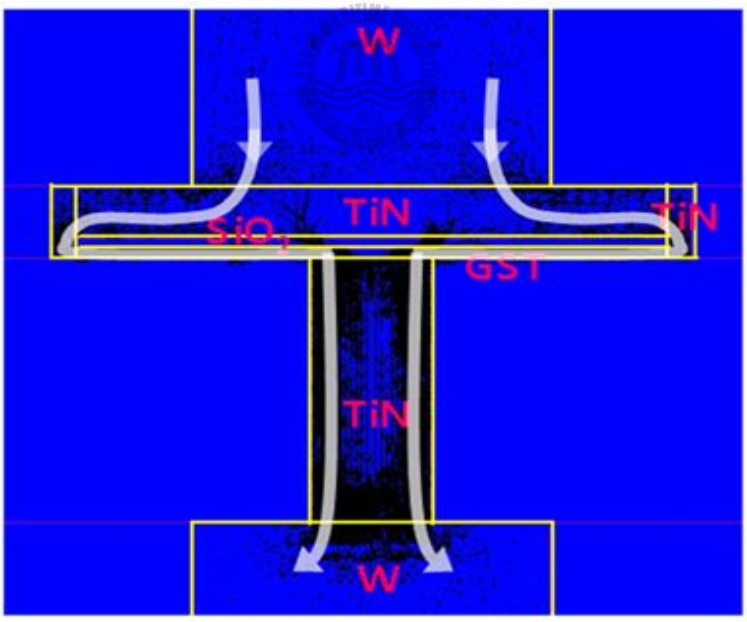
Fig. 4.18 Schematic diagram of planar type PRAM with heat blocking layer

However in novel PRAM cell, dielectric layer SiO_2 was deposited on the top of phase change material for complement which is heat to prevent to give off to top electrode.

At this time, as only SiO_2 on the top was, the current couldn't pass. So TiN was deposited at the edge of multi-layer. Fig. 4. 19 shows the path of current flow with conventional PRAM cell and novel structure PRAM cell.



(a) Conventional PRAM unit cell



(b) Novel structure PRAM unit cell

Fig. 4.19 Current flow with each structure PRAM unit cell

We investigated temperature and reset current of planar type PRAM cell with heat blocking layer using 3-D finite element analysis. Fig. 4.20 shows that comparison of novel structure and conventional structure.

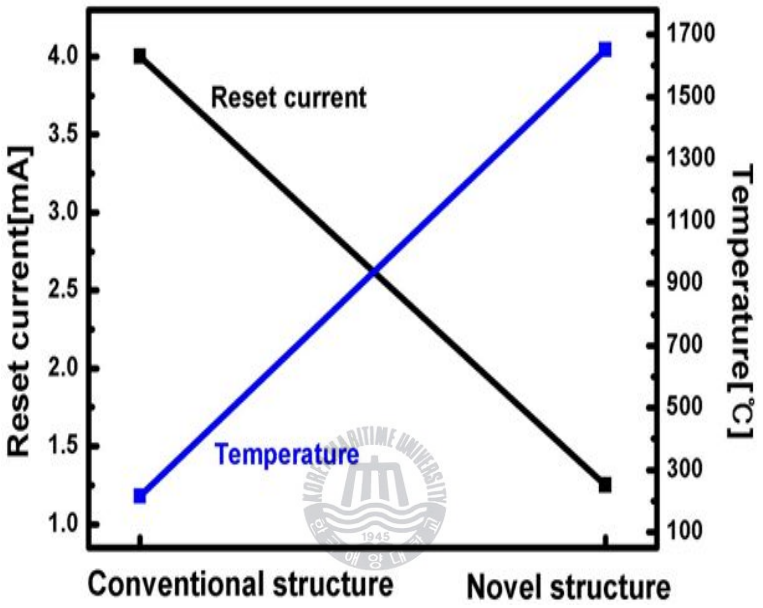


Fig. 4.20 Temperature and reset current of planar type PRAM cell with each structure

As this figure the reset current extremely decreased 68% and the temperature increased 660% at 10 nm thickness of GST. From this result, heat blocking layer works well for planar type PRAM cell.

Chapter 5. Conclusion

Today, the market for non-volatile memory is dominated by the Flash technology. Due to the increasing cost of down scaling Flash technology, the memory industry is searching for alternative memory concept. One of most promising candidates is the electrical phase change technology PRAM.

In this paper, we fabricated the PRAM unit cell and investigated electro and thermal characteristics of PRAM unit cell with novel structure using SiO_2 heat blocking layer.

As thickness of GST thin film decreased from 400 ㎚ to 300 ㎚, reset current and temperature changed a bit but did not affect so much memory cell operation. But as thickness of GST thin decreased from 300 ㎚ to 200 ㎚, reset current increased from 15 ㎃ to 17.4 ㎃ and temperature decreased from 704.86 ℃ to 536.60 ℃. As reset current and temperature changed like at 200 ㎚ thickness of GST thin film, the memory cell operation did not work as normal. From this results, we investigated material parameters of heater electrode for why reset current and temperature changed. After investigation, we found that heat which was generated between phase change material GST and heater electrode TiN was given to top electrode W due to thin thickness of GST thin film.

We have throughly investigated the decreasing of temperature

of 200 ㎚ thickness of GST thin film and found that the severe heat loss occurred at top electrode. In the case of 200 ㎚ thickness of GST thin film, a heat rapidly transferred to top electrode before melting temperature. A heat which contacted with top electrode transferred easily to outside and temperature decreased. Therefore, novel structure PRAM which deposited SiO_2 blocking layer instead of part of top electrode was proposed. The SiO_2 blocking layer which is dielectric layer can protect the heat to give off through top electrode.

In comparison with conventional PRAM at 200 ㎚ GST thin film thickness, temperature of novel structure PRAM highly increased from 536.60 ℃ to 817 ℃ and reset current of novel structure PRAM decreased abruptly. from 17.4 ㎃ to 13.7 ㎃. This result shows that novel SiO_2 blocking layer of PRAM successfully protected heat to give off to top electrode.

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